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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,754	02/02/2001	Ming-Dou Ker	H000039	6902

27760 7590 12/03/2001

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EXAMINER	
SEFER, AHMED N	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/03/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,754	KER ET AL.	
	Examiner	Art Unit	
	Ahmed N Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 and 5-19 is/are rejected.

7)☐ Claim(s) 4 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The formation of first and second channel regions with different lengths disposed between first and second regions of said first MOS transistor is not clearly disclosed in the specification. Without this information it would take undue experimentation to make and use the claimed invention.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 7 and 14 recite the limitation "said MOS transistor". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Ker et al. US Patent No. 5,637,900.

Ker et al disclose (see fig. 8) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a first region 623 of a second conductivity type within said substrate for forming a drain of a first MOS transistor P2; a second region 620 of the second conductivity type within said substrate for forming a source of the first MOS transistor; a third region of the second conductivity type 630 within said substrate coupled to a gate of a second MOS transistor P5, wherein a fourth region 720 of first conductivity type is disposed adjacent to the third region of the second conductivity type for surrounding said first MOS transistor with an additional pick-up diffusion to reduce a turn-on speed or/and a longer channel length to increase a drain-base breakdown voltage of said first MOS transistor (as in claim 2).

8. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Ker et al. US Patent No. 5,637,900.

Ker et al disclose in fig. 8 a semiconductor structure for electrostatic discharge

(ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a pair of first regions 620/623 of a second conductivity type within said substrate for defining a first channel region 810 of the second conductivity type for a first MOS transistor P2; and a pair of second regions 650 of a second conductivity type within said substrate for defining a second channel region 820 of the second conductivity type for a second MOS transistor P5, wherein the channel length of said first channel region is greater than the channel length of said second channel region to reduce a turn-on speed of said first MOS transistor.

9. Claims 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ker et al. US Patent No. 5,637,900.

Ker et al disclose (see fig. 8 and col. 12, lines 10-13) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a p-type substrate of forming a base for said semiconductor structure; a first N+ region 623 within said substrate for forming a drain of a first MOS transistor P2; a second N+ region 620 within said substrate for forming a source of the first MOS transistor; a third N+ region 630 within said substrate coupled to a gate of a second MOS transistor P5, wherein a P+ region 720 of first conductivity type is disposed adjacent to the third region of the second conductivity type for surrounding said first MOS transistor with an additional pick-up diffusion to reduce a turn-on speed or/and a longer channel length to increase a drain-base breakdown voltage of said first MOS transistor (as in claim 9).

10. Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Ker et al. US Patent No. 5,637,900.

Ker et al disclose (see fig. 8 and col. 12, lines 10-13 a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a p-type substrate forming a base for said semiconductor structure; a pair of first N+ regions 620/623 within said substrate for defining a first n-channel region 810 for a first MOS transistor P2; and a pair of second N+ regions 650 within said substrate for defining a second n-channel region 820 for a second MOS transistor P5, wherein the channel length of said first channel region is greater than the channel length of said second channel region to reduce a turn-on speed of said first MOS transistor.

11. Claims 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Ker et al. US Patent No. 5,637,900.

Ker et al disclose (see figs. 6 and 8) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit, said semiconductor structure connected between an input pad and an internal circuit of said integrated circuit and comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a first channel 810 of a second conductivity type formed between first regions 630/620 of said second conductivity type within said substrate for a first MOS transistor P3 or first MOS transistor P3 which is stacked on a third MOSFET P2 of a second conductivity type (as in claim 17); and a second channel 820 of a second conductivity type formed between first regions 650 of said second

conductivity type within said substrate for a second MOS transistor P5 or a second MOS transistor P5 which is stacked on a fourth MOSFET P4 of a second conductivity type (as in claim 17), wherein the channel length of said first channel is greater than the channel length of said second channel (as in claims 16 and 18), wherein an additional pick diffusion region 720 is disposed adjacent to said first regions of second conductivity type to reduce a turn-on speed or increase a drain breakdown voltage of first MOS transistor.

12. Claim 19 is rejected under 35 U.S.C. 102(b) as being anticipated by Ker et al. US Patent No. 5,637,900.

Ker et al disclose (see fig. 6) a semiconductor structure for electrostatic discharge (ESD) protection, comprising at least one ESD protection device P3; and at least one guarded device P1 which is turned-on by a turn-on restrain means, wherein the ESD protection device can be turned-on before the guarded device is turned on.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 3, 6, 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. US Patent No. 5,637,900 in view of admitted prior art (APA).

Ker et al disclose all the claimed subject matter but fail to teach a pre-puffer circuit coupled to a gate of MOS transistor or a channel and an output pad coupled to a first region or regions of a MOS transistor.

The APA disclose in fig. 5 a pre-puffer coupled to a gate of a MOS transistor or indirectly to a channel; and an output pad coupled to a region or regions of a MOS transistor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of the APA with Ker et al, since that would reduce transient contributions to a response.

Allowable Subject Matter

15. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ahmed N Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
November 18, 2001